

REMARKS

Claims 18, 20, 21 and 24 to 26 have been amended for improved accuracy or to present allowable claims in independent form. Claims 1 to 30 remain active of which claims 1 to 17 and 28 to 30 have been allowed and claims 20 to 25 have been indicated to be allowable and were objected to as depending from a rejected claim.

Claims 18 and 19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (U.S. 6,297,082) in view of Nakahara (U.S. 5,075,242). The rejection is again respectfully traversed.

Claim 18 provides a method of semiconductor fabrication wherein source/drain regions in one high voltage transistor are implanted using a threshold voltage adjust implantation which is concurrently also being used to adjust the threshold voltage of another relatively low voltage transistor. This is set forth in claim 18 by the language adjusting a threshold voltage of a first transistor relatively low voltage device in a first region of said semiconductor device substrate and, concurrently with the step of adjusting, forming a source/drain region of a second transistor relatively high voltage device, both using the same implant. Clearly, Lin et al. does not teach or suggest the problem or the solution thereof as admitted in the Office action. In fact, the Examiner states that Lin adjusts the threshold voltage of the low voltage device with a different implantation than is used to form the source/drain region of the high voltage device. Nakahara also fails to teach or suggest the above described concept, even were Nakahara to be combinable with Lin et al., which it is not. In fact, Nakahara does not even discuss fabrication of a semiconductor device wherein concurrent fabrication steps for fabrication of a relatively high voltage transistor and a relatively low voltage transistor are provided.

The fact that identical or similar (as opposed to a high voltage and low voltage device) devices are fabricated using a concurrent implantation has nothing whatsoever to do with the problem solved by the claimed invention. It follows that anyClearly, therefore, there are no fabrication steps involving the specific types of fabrication steps claimed. Furthermore, as stated above, there can be no teaching or suggestion to combine the references when neither reference even teaches or suggests the problem solved by the present invention, let alone the solution thereto.

Claim 19 depends from claim 18 and therefore defines patentably over the applied references for at least the reasons presented above with reference to claim 18.

In addition, claim 19 further limits claim 18 by requiring the step of forming a source/drain region of the first transistor device. No such combination is taught or suggested by Lin et al., Nakahara or any proper combination of these references.

Claim 26 requires, among other steps, the steps of selectively concurrently implanting a first relatively low voltage transistor region in said semiconductor device substrate to adjust a threshold voltage associated with a first transistor device and a portion of a second transistor region to form a source/drain region associated with a second relatively high voltage transistor device. The arguments presented above with reference to claim 18 apply and are incorporated by reference.

Claim 27 depends from claim 26 and therefore defines patentably over the applied references for at least the reasons presented above with reference to claim 26.

In addition, claim 27 further limits claim 26 by requiring thatselectively implanting the first transistor region and a portion of the second transistor region include the step of implanting one of phosphorus, arsenic and boron in the first transistor region

and a portion of the second transistor region. No such combination is taught or suggested by Lin et al., Nakahara or any proper combination of these references.

In view of the above remarks, favorable reconsideration and allowance are respectfully requested.

Respectfully submitted,



Jay M. Cantor
Reg. No. 19906
(202) 639-7713